IN THE SPECIFICATION

Please amend the paragraph beginning at page 8, line 11, as follows:

A small-signal equivalent circuit of the novel bypass network is shown in FIG. 4A. In this schematic, Rsw is the MOS switch resistance, while Cbin, Cout, and Ccol are the total parasitic capacitances at the input base, output, and collector nodes, respectively. This network can be simplified to that shown in FIG. 4B by assuming that the switch impedance is low (i.e., Rsw -> 0); thus, CM is shorted out, while all of the on-chip parasitic capacitance can be lumped together into Ctot, which is now in parallel with LM. The entire on-chip portion of the LNA then behaves as a single parallel resonant circuit. Realizing the 50-ohm match therefore involves the tuning of this parallel resonant circuit together with the input matching network. The tuning of the parallel resonant circuit is realized by scaling the sizes of the bypass transistors.